

UPPAAL Tutorial

Times - a Tool for Implementation
and Modelling of Embedded
System

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RTSS'05

Real-Time Programs

Plant
Continuous

Controller Program
Discrete

sensors actuators

- Consists of a set of tasks
- Activated by sensor or timer event
- **Central Problem:** Scheduling of tasks
- Rate-Monotonic Analysis [LL'73], EDF, ...
- Response-Time Analysis [JP'86]
- Earliest-Deadline First...



Classical vs. Automata-based Approach

Classic Scheduling Theory

- Periodic Tasks
- Well studied algorithms
- Efficient
- Pessimistic (when tasks are not periodic)
- Extensions for sporadic, jitter, etc.

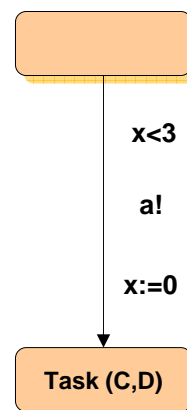
Automata-based Approach

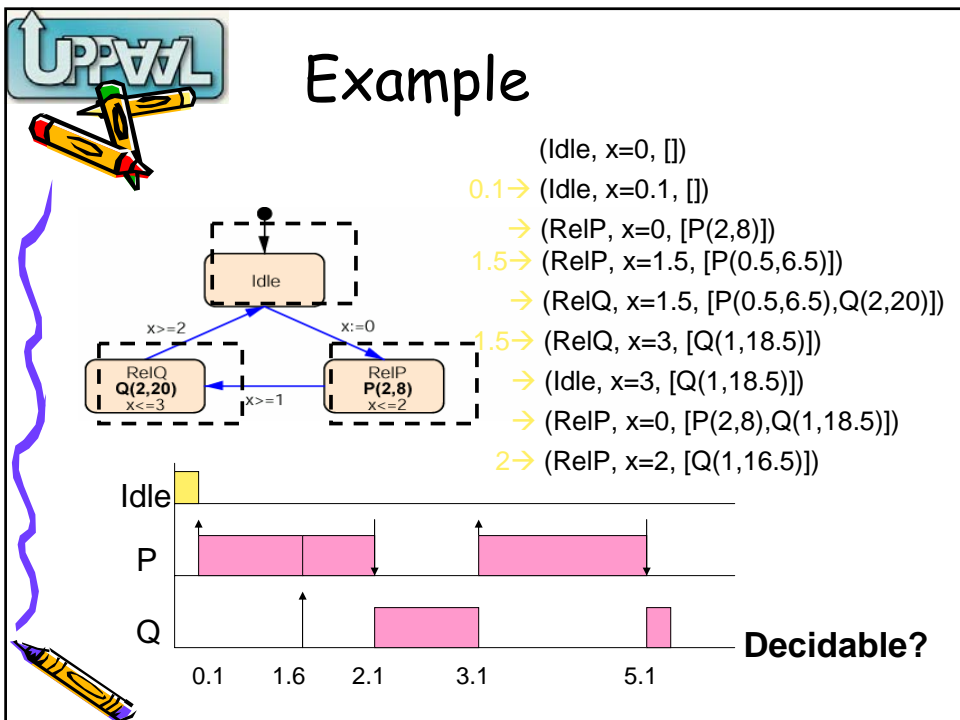
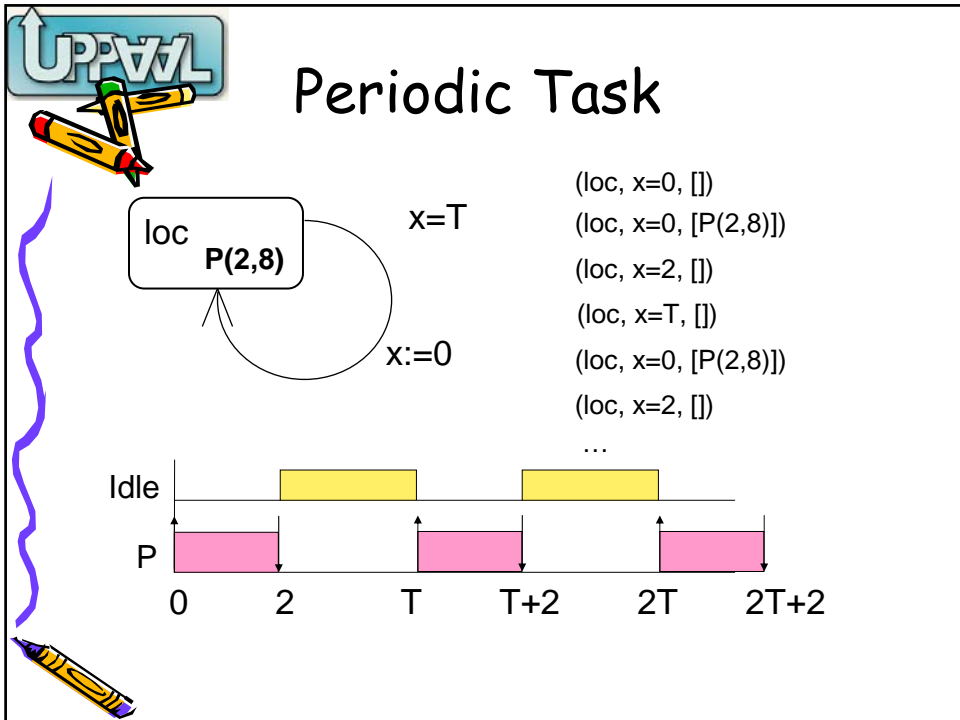
- Automata used to describe task arrival
- General release patterns
- Precise
- Schedulability?
- Decidability?
- Efficiency?

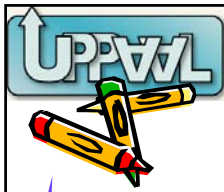


Timed Automata with Tasks

- Events
 - synchronization
 - interrupts
- Timing constraints
 - specifying event arrivals
 - e.g. periodic or sporadic
- Tasks (executable programs)
 - asynchronous execution
 - interrupt processing
 - internal computation



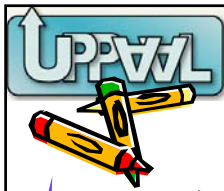




Schedulability Analysis

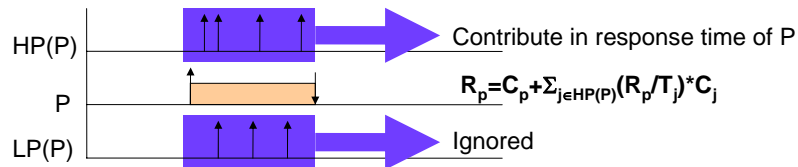
- All tasks meet their deadlines?
- FACT [Wall, Yi, 1998]
 - The schedulability problem is **decidable** for **non-preemptive** tasks.
- Conjecture [since 1998]
 - The schedulability problem is **undecidable** for **preemptive** tasks.
- FACT [TACAS 2001]
 - The Schedulability Problem **is decidable for preemptive tasks.**

WRONG!



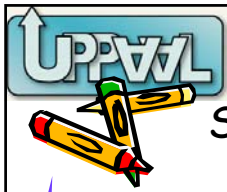
Efficiency [TACAS'03]

- High complexity for the **general case, e.g. EDF**
- 2 clocks for each task instance n_i of a task type
- Number of clocks for EDF: $2\sum_i n_i$
- For fixed priorities the analysis is similar to Response Time Analysis (Joseph, Pandya):



- For fixed priority systems only **two** clocks are needed for schedulability analysis!



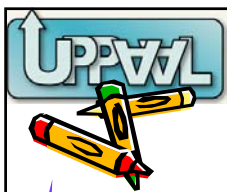


TIMES - Tool for Automatic Schedulability Analysis and Code Synthesis

The screenshot shows the TIMES tool interface. The main window displays a state transition diagram with states like 'FINISHED', 'IDLE', and 'REC_TASK_A'. A 'Status' window shows variables like 'Autoaton_A.x = 0' and 'i = 4'. A 'WCR Analysis' window displays a table of Worst Case Response Times for tasks A, B, C, and D.

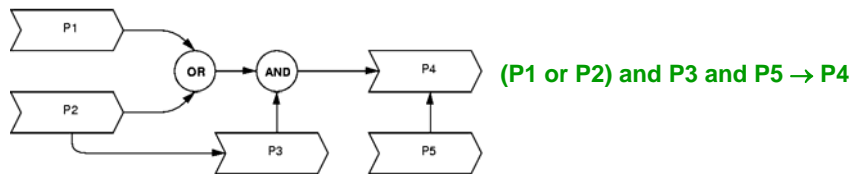
Name	C	WCRT	D
task_A	1	1	3
task_B	5	8	20
task_C	10	20	25
task_D	5	30	30

- Timed Automata with Tasks
 - FPS, EDF, ...
 - Shared resources (Priority Ceiling Protocol)
- Analysis:
 - Schedulability
 - Response-time
 - Model-checking
- Simulation with MSC and Gantt-charts
- Code synthesis

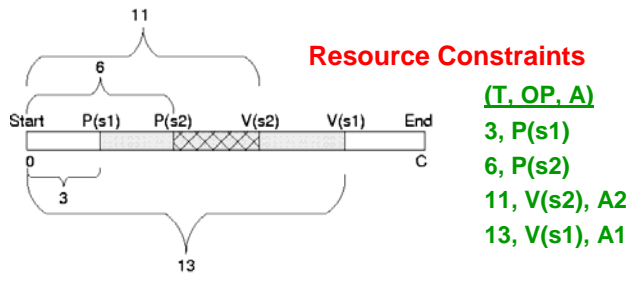


Extensions [NJC'04]

Precedence Constraints



Resource Constraints



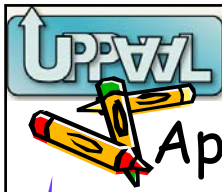
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TIMES DEMO

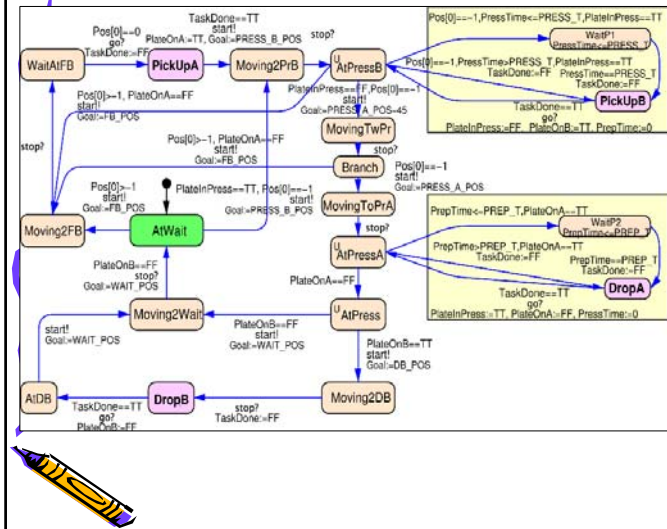
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Production Cell [NJC'03]

- Academic example
- LEGO Hitachi H8 processor
- brickOS operating system
- 15 tasks
- Task code written in C



Application: Production Cell



- System:**
- 15 tasks
 - Hitachi H8
 - Task code in C
- Analysis:**
- 9 sec and 13 MB using over-approximation
 - Identified dead code
- Synthesis:**
- 550 lines of C-code excl. task code
 - Executed on hardware